FIG.1

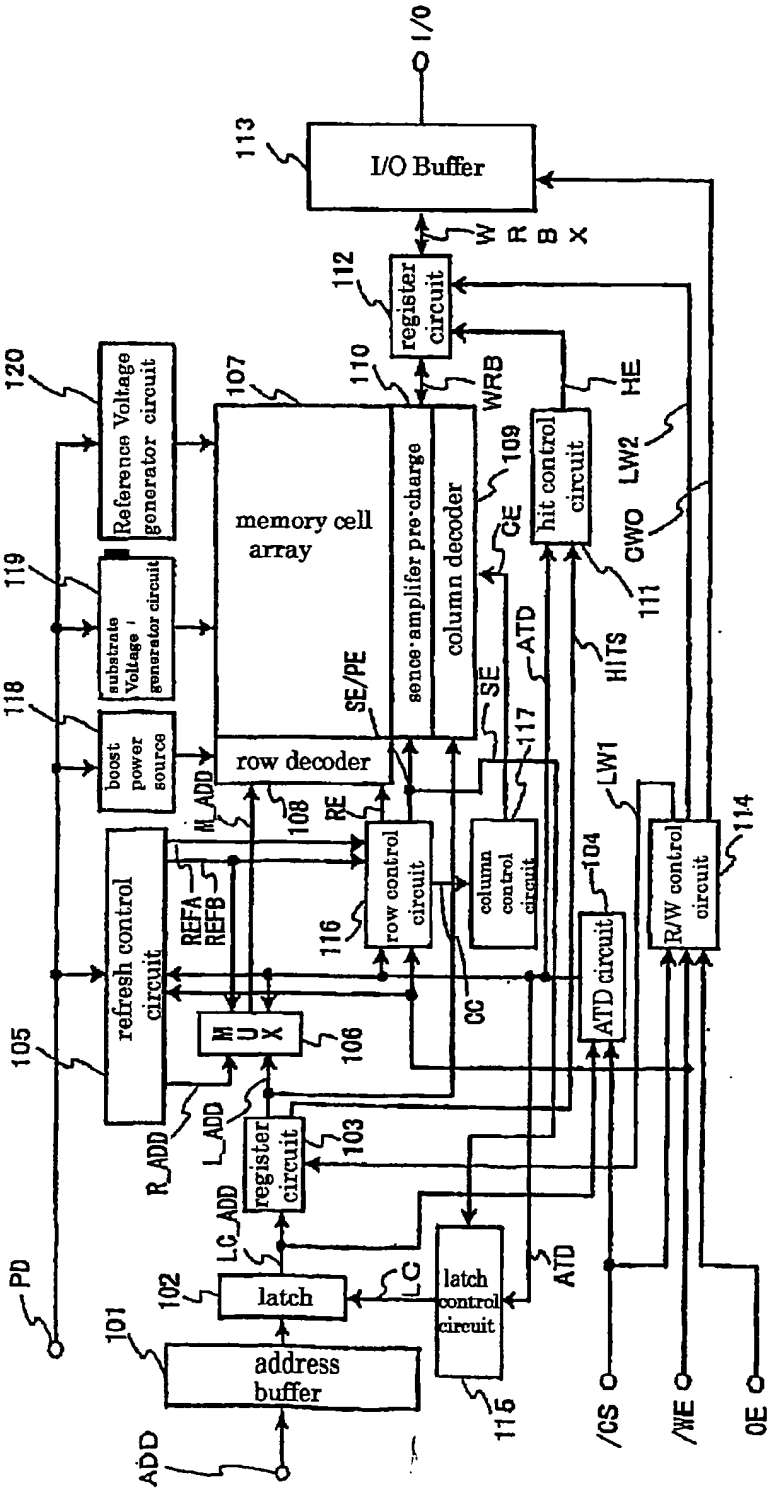

FIG.2

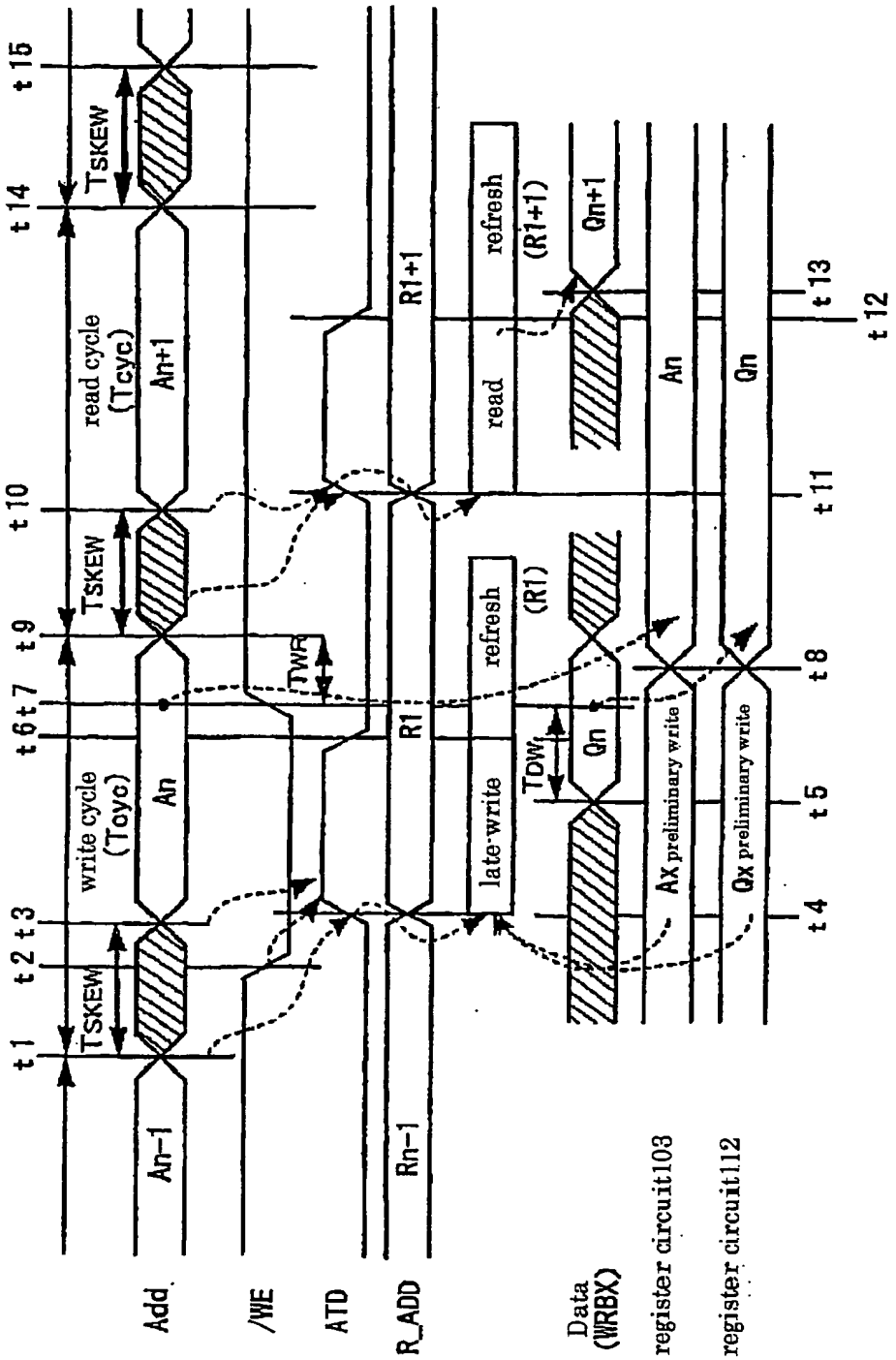
t15
t14
t10
t9
t6 t7
t2 t3
t1
t13
t12
t11
t8
t5
t4
TSKEW
TSKEW
TSKEW
TWR
TDW
read cycle (Tcyc)
write cycle (Toyc)
An+1
An
An-1
R1+1
R1
Rn-1
refresh (R1+1)
read
refresh (R1)
late-write
Qn+1
Qn
An
Qn
AX preliminary write
QX preliminary write
Add
/WE
ATD
R_ADD
Data (WRBX)
register circuit103
register circuit112

FIG.3

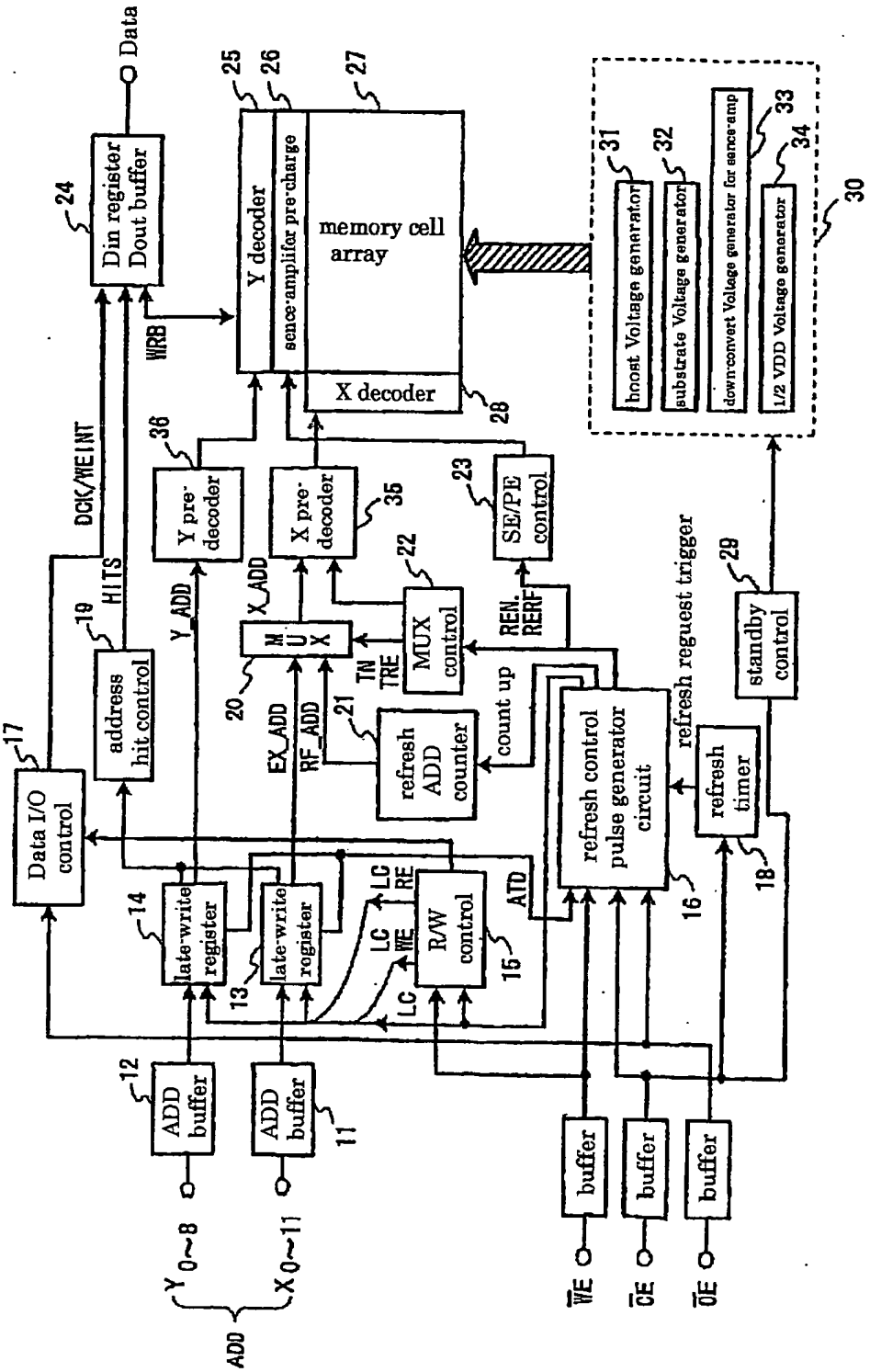
Data
Din register Dout buffer
24
25
26
27
Y decoder
sence-amplifier pre-charge
memory cell array
X decoder
28
WRB
DCK/WEINT
HITS
19
address hit control
17
Data I/O control
Y pre-decoder
36
X pre-decoder
35
23
SE/PE control
22
MUX control
REN.
RERF
TN
TRE
M U X
20
X_ADD
Y_ADD
EX_ADD
RF_ADD
21
refresh ADD counter
count up
refresh control pulse generator circuit
refresh reguest trigger
refresh timer
18
standby control
29
16
late-write register
14
late-write register
13
LC
WE
LC
RE
LC
R/W control
15
ATD
ADD buffer
12
ADD buffer
11
Y 0~8
X 0~11
ADD
buffer
buffer
buffer
WE
CE
OE
30
boost Voltage generator
31
substrate Voltage generator
32
down-convert Voltage generator for sence-amp
33
1/2 VDD Voltage generator
34

FIG.4

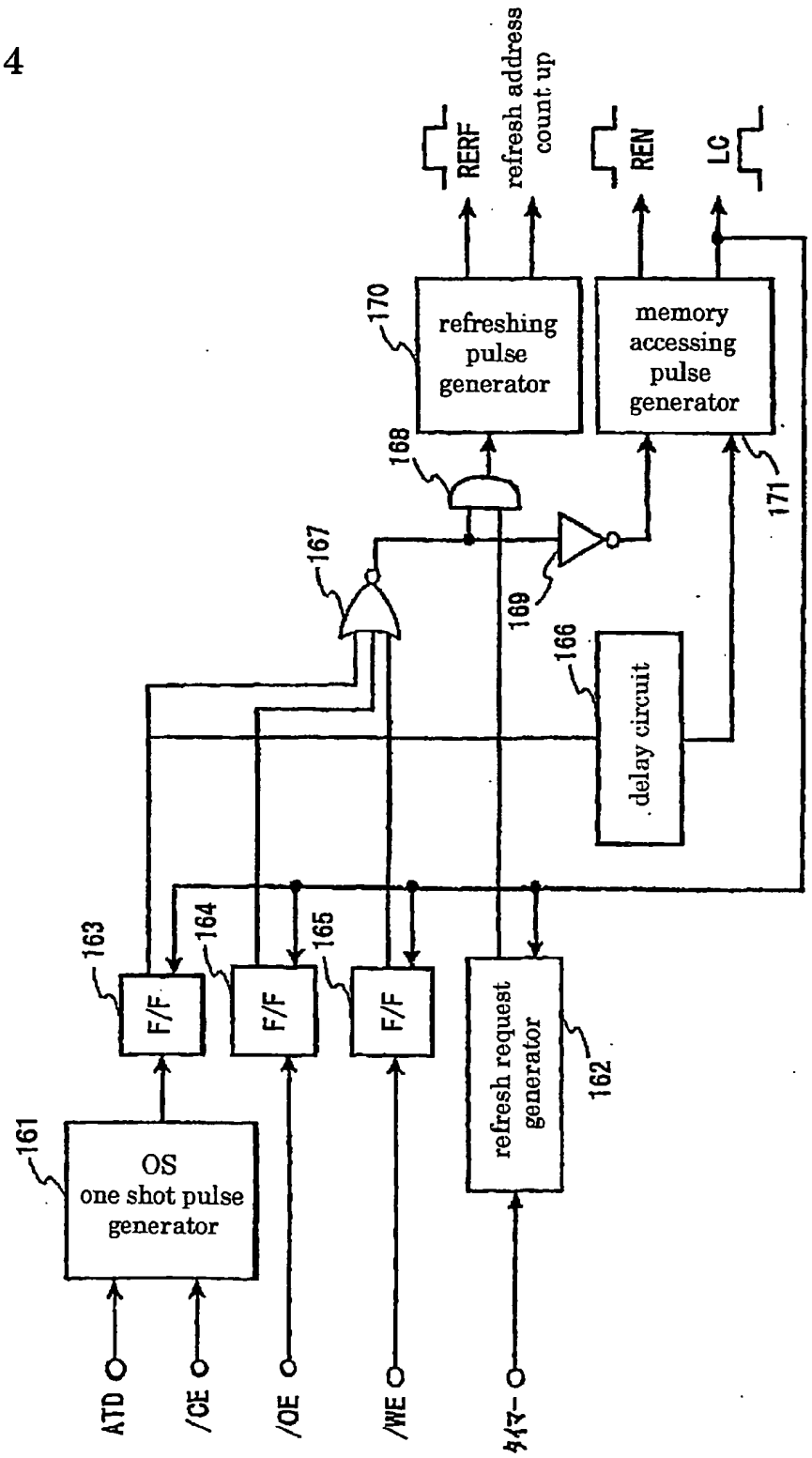

FIG.5

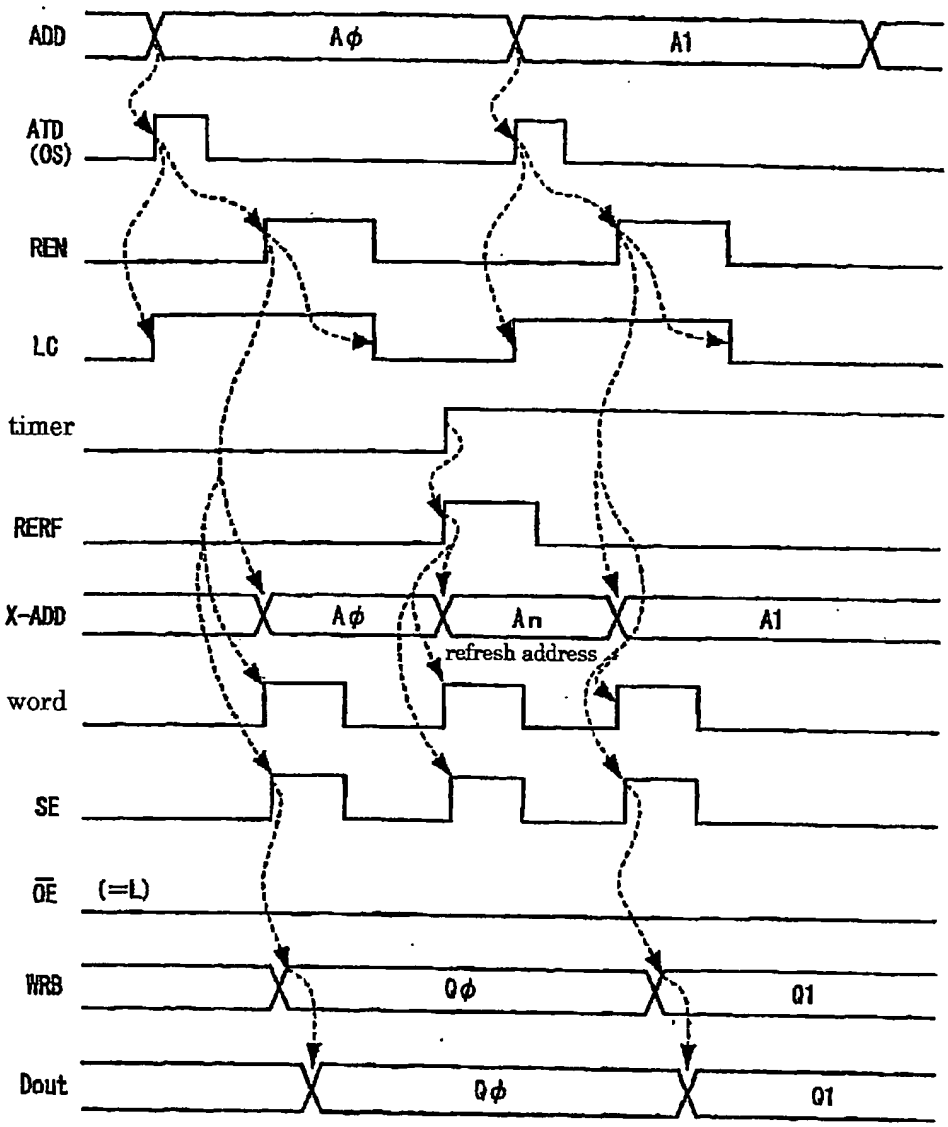

FIG.6

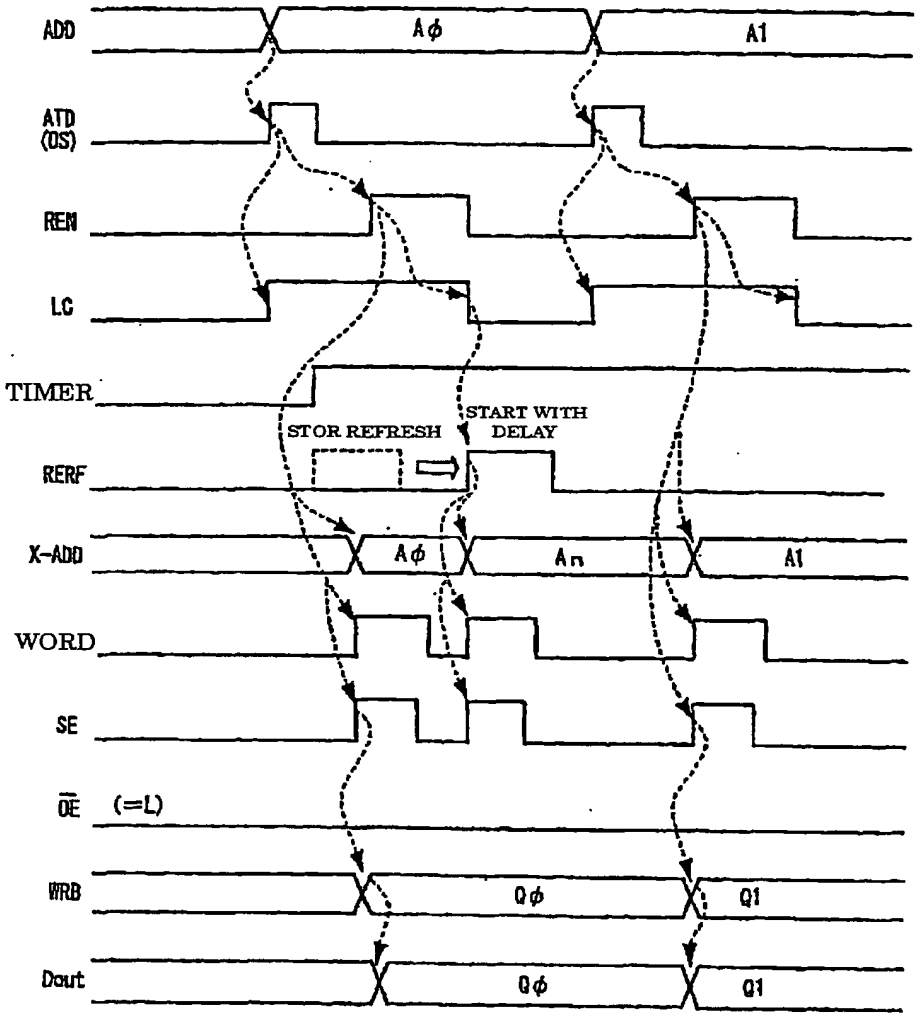

FIG.7

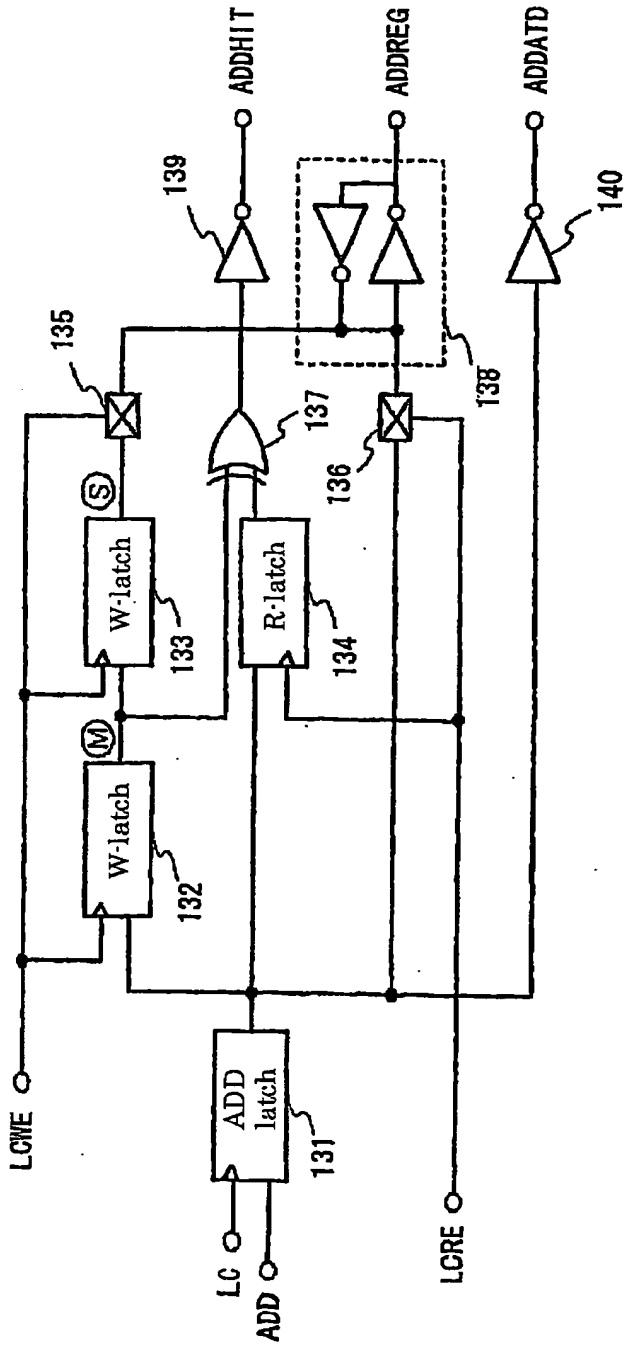

FIG.8

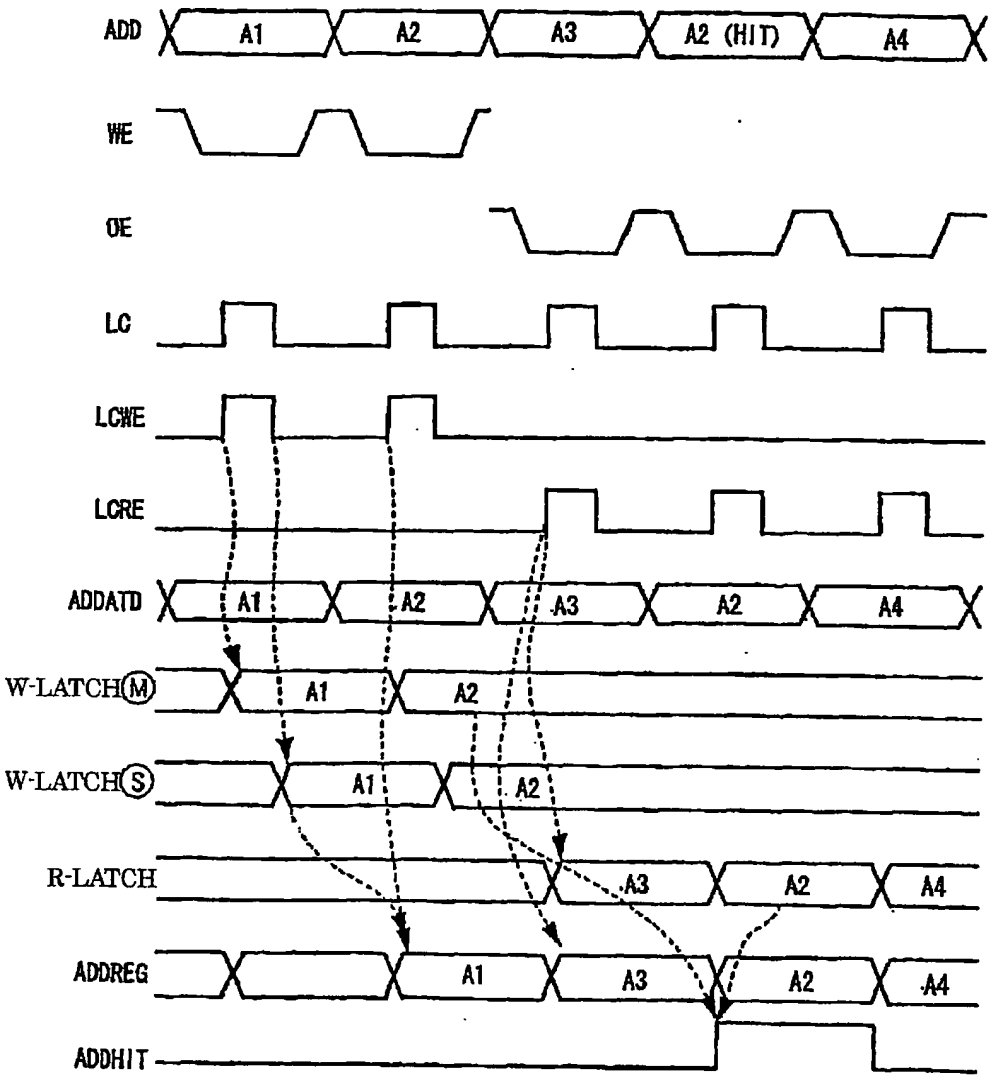
ADD
A1
A2
A3
A2 (HIT)
A4
WE
OE
LC
LCWE
LCRE
ADDATD
A1
A2
A3
A2
A4
W-LATCH(M)
A1
A2
W-LATCH(S)
A1
A2
R-LATCH
A3
A2
A4
ADDREG
A1
A3
A2
A4
ADDHIT

FIG.9

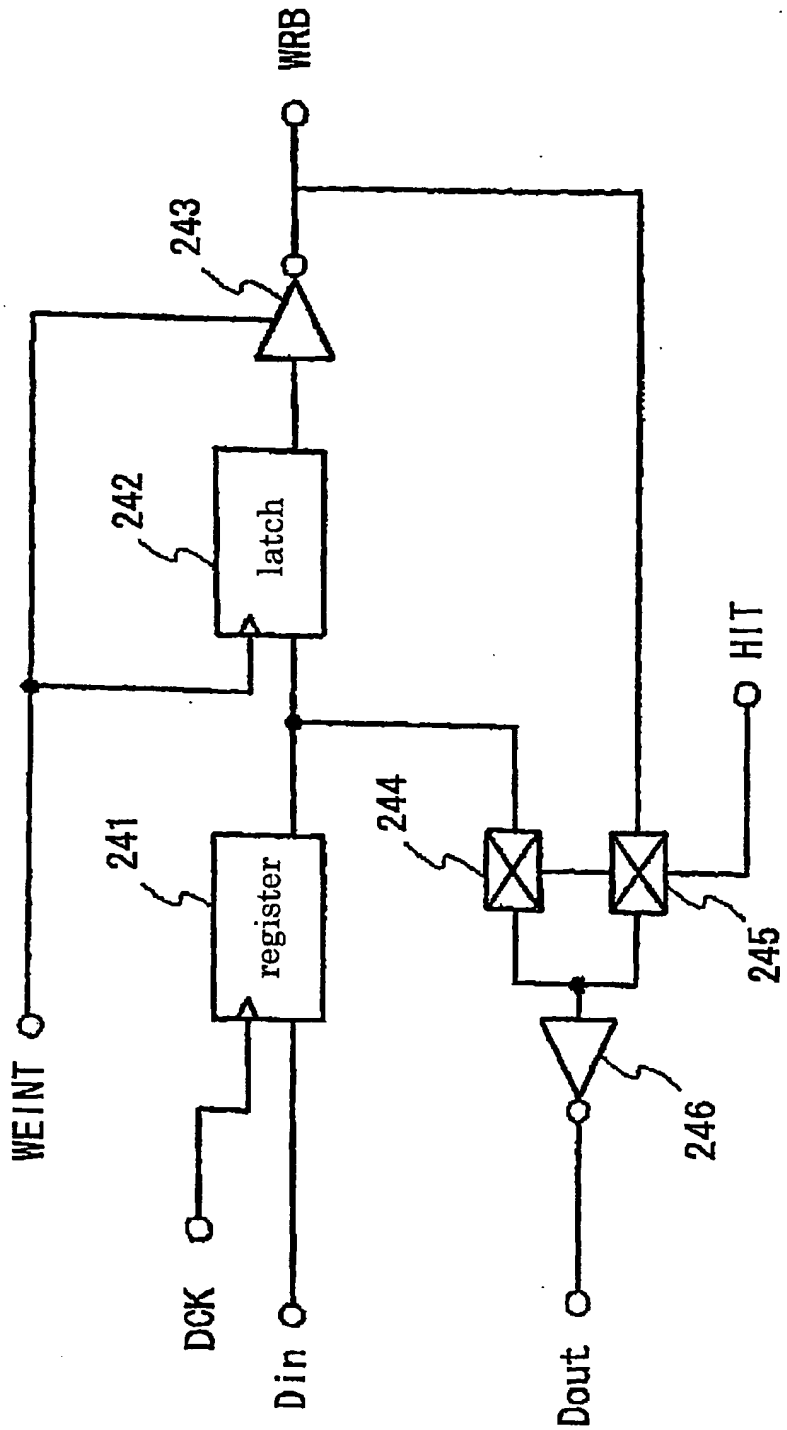

FIG.10

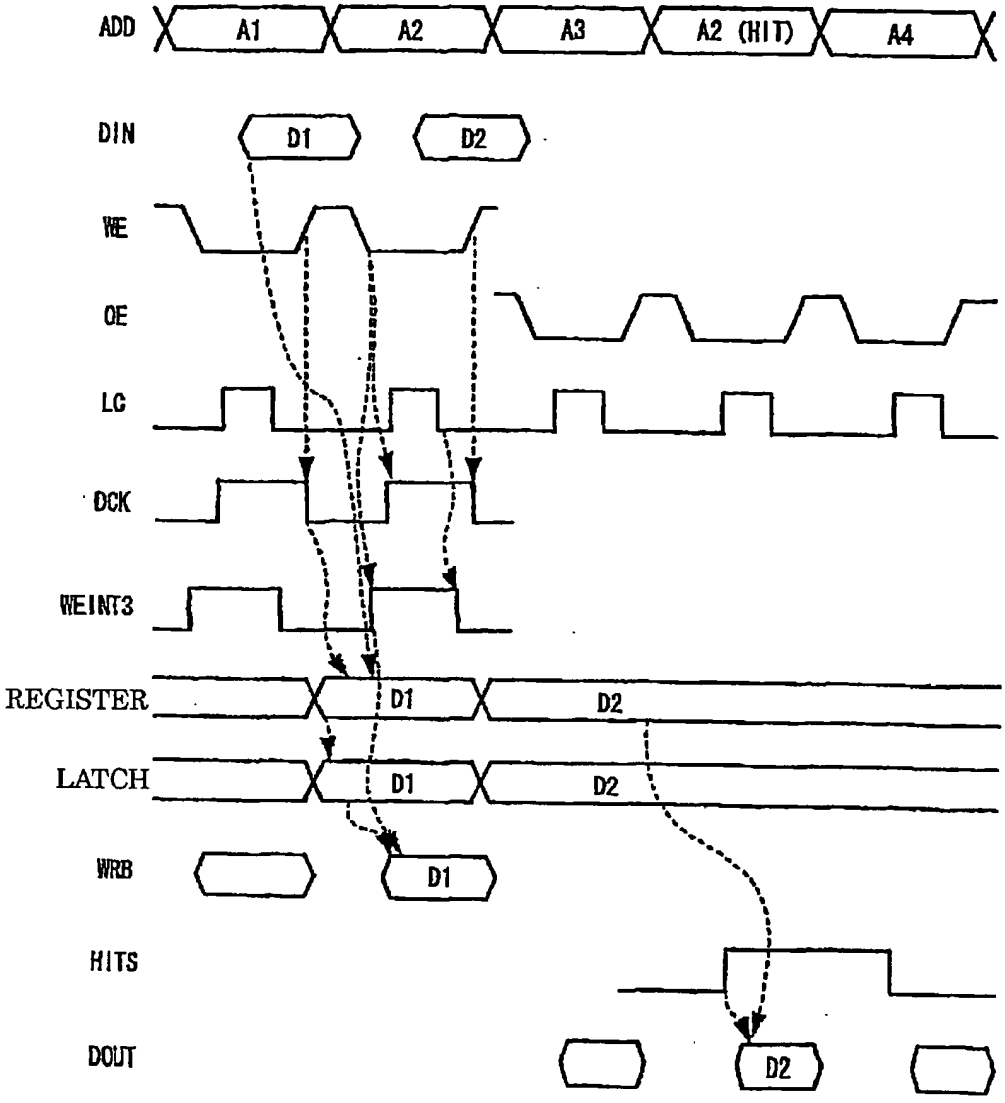

FIG.11

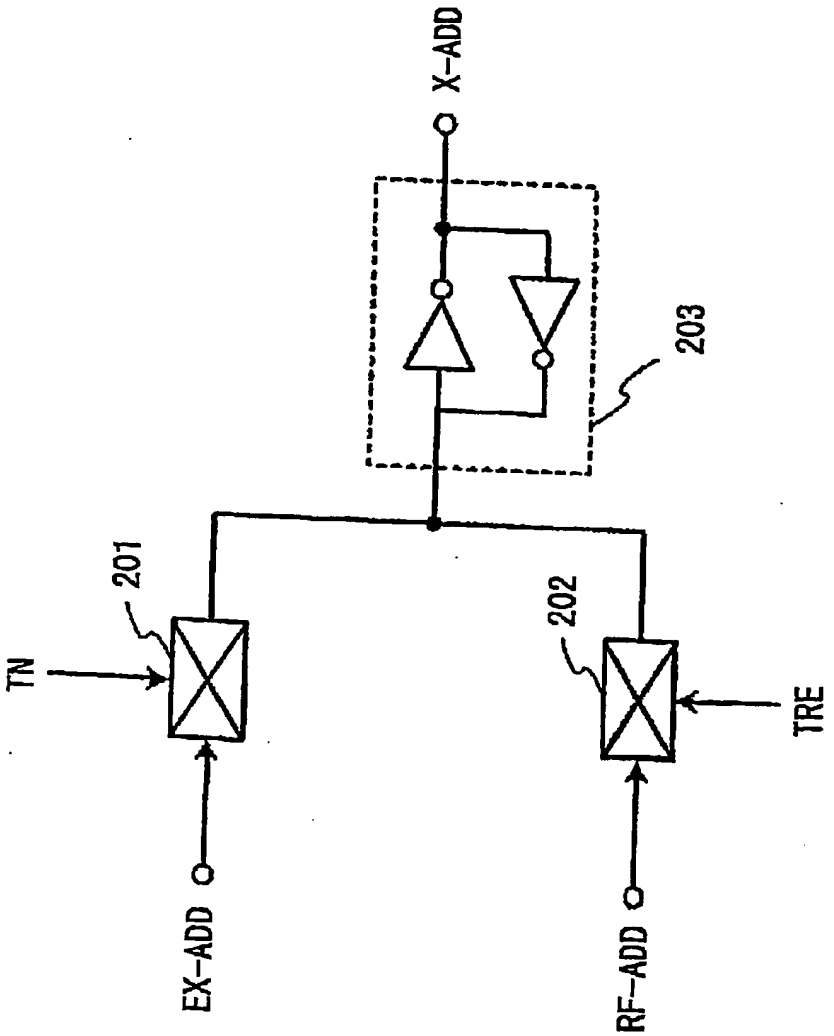

FIG.12

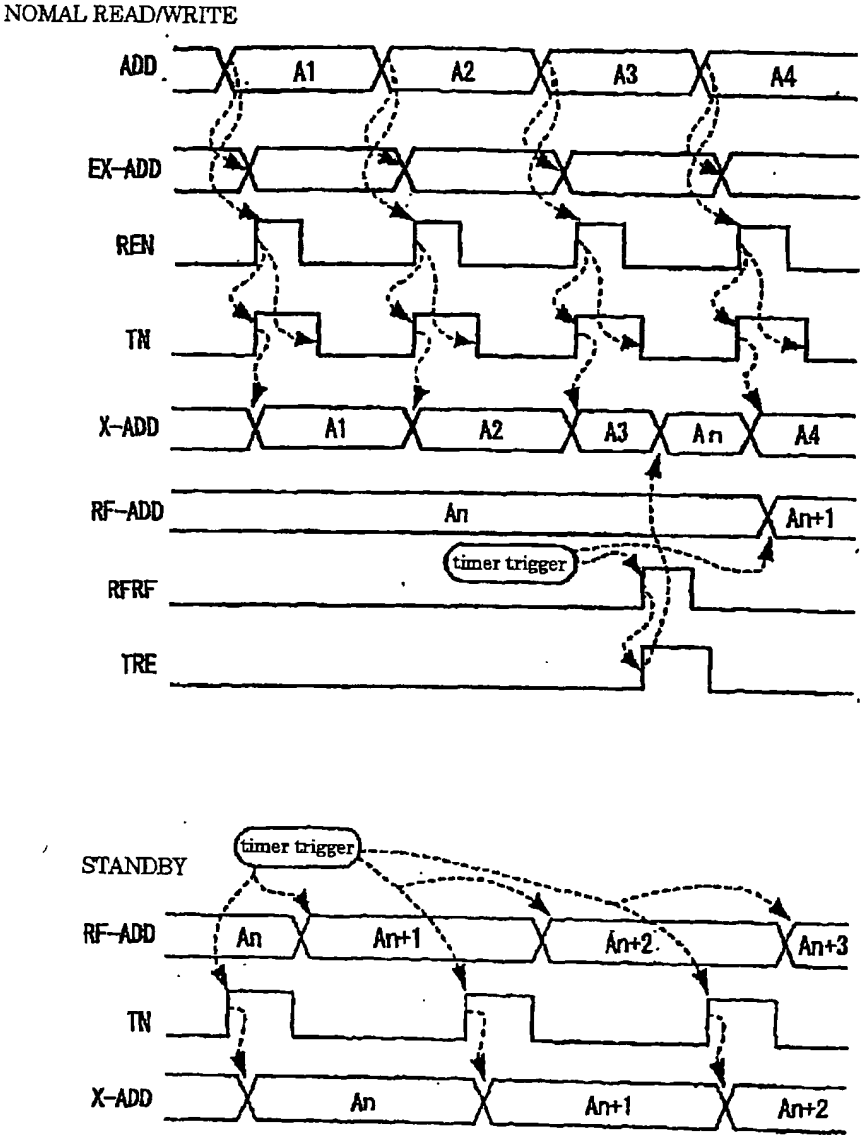

FIG.13

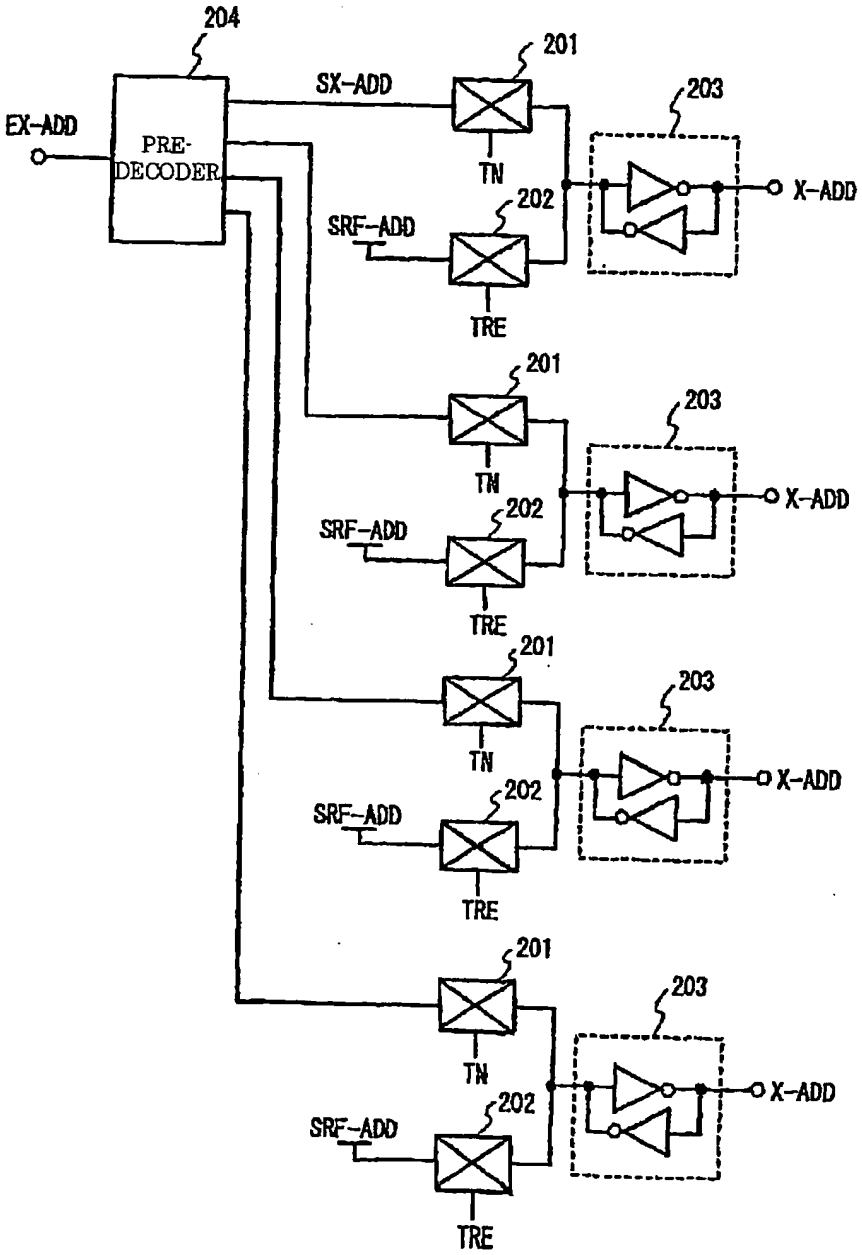

FIG.14

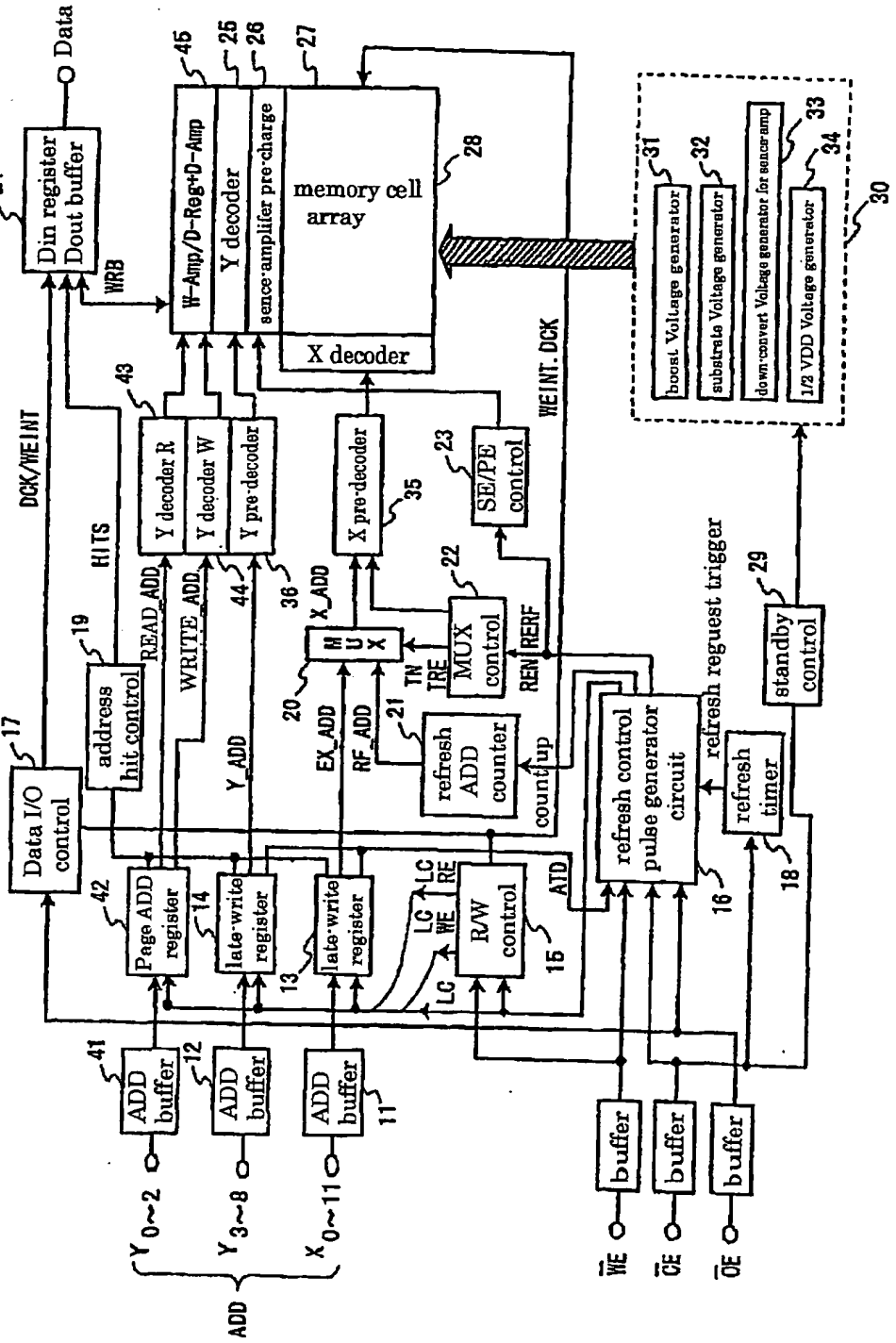
Data
Din register
Dout buffer
WRB
W-Amp/D-Reg+D-Amp
Y decoder
sence-amplifer pre-charge
memory cell array
X decoder
boost Voltage generator
substrate Voltage generator
down-convert Voltage generator for sence-amp
1/2 VDD Voltage generator
WEINT. DCK
DCK/WEINT
HITS
Y decoder R
Y decoder W
Y pre-decoder
X pre-decoder
SE/PE control
READ_ADD
WRITE_ADD
Y_ADD
X_ADD
EX_ADD
RF_ADD
MUX
MUX control
TN
IRE
REN
RENF
address hit control
refresh ADD counter
count up
refresh control pulse generator circuit
refresh request trigger
refresh timer
standby control
Data I/O control
Page ADD register
late-write register
late-write register
R/W control
LC
WE
RE
ATD
ADD buffer
ADD buffer
ADD buffer
buffer
buffer
buffer
Y0~2
Y3~8
X0~11
ADD
WE
CE
OE

FIG.15

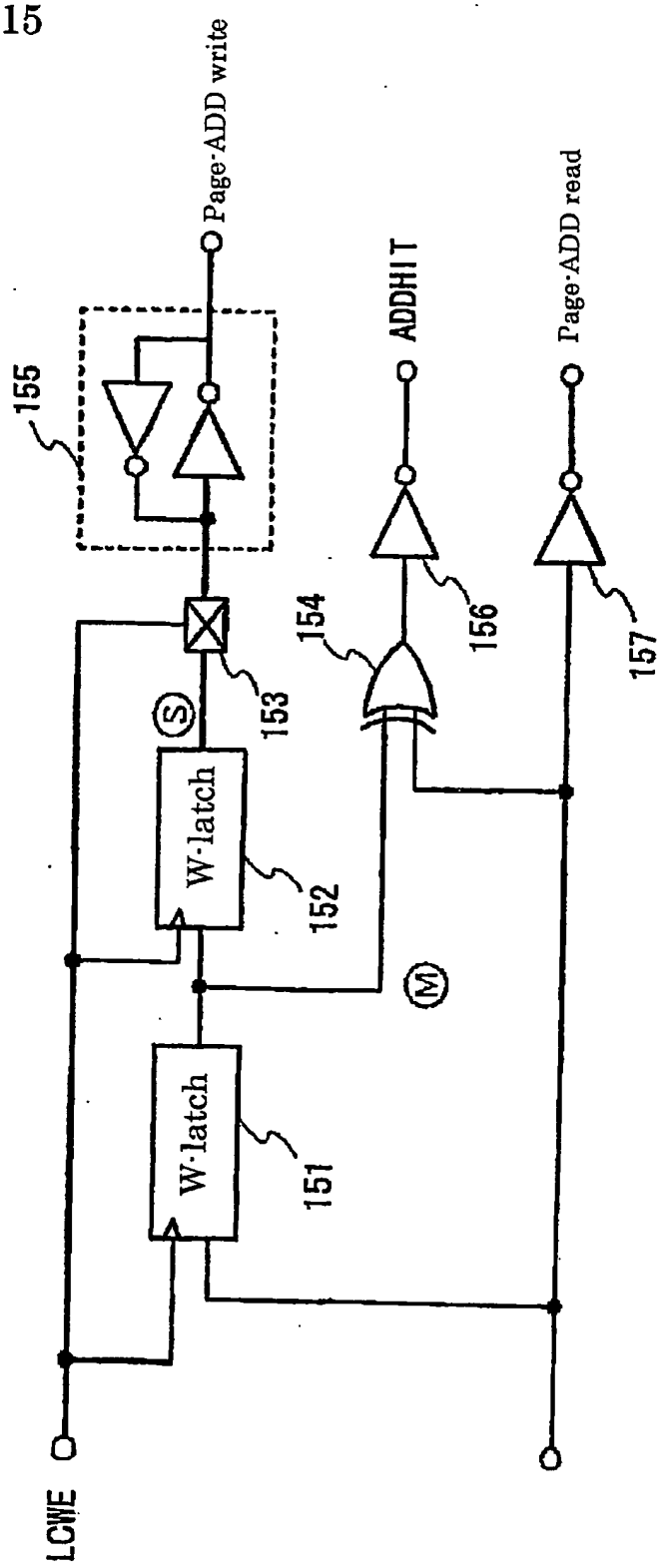

FIG.16

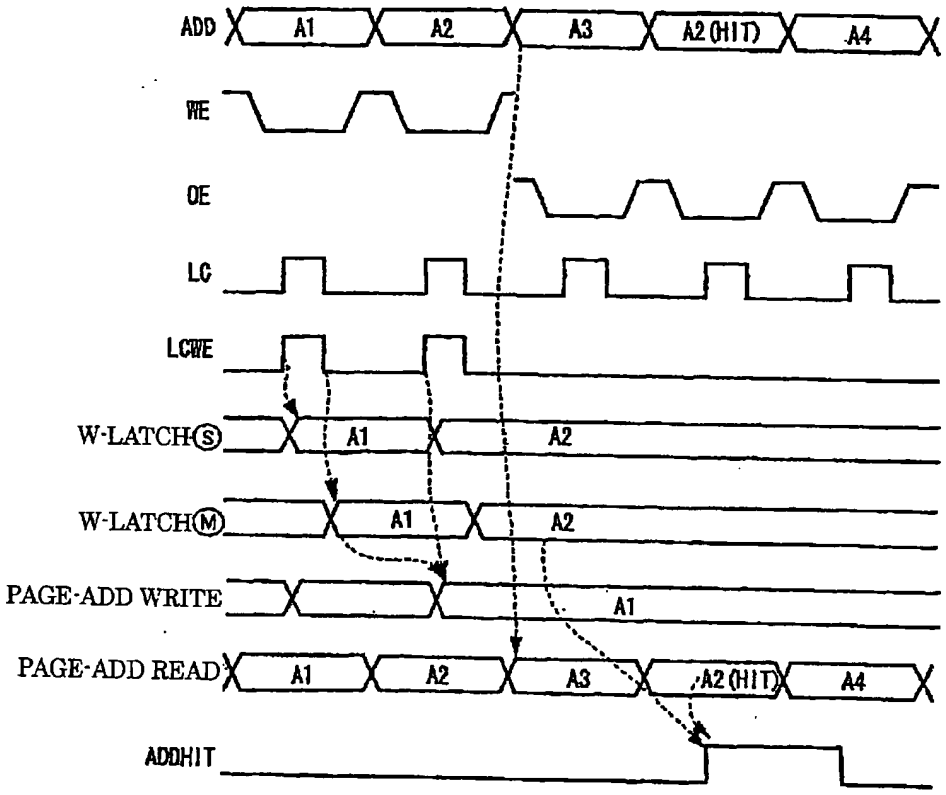

FIG.17